ABSTRACT

Methods of testing scan chains in integrated circuits are provided. One method may include steps of placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain, placing the scan chain circuit into a failing region, applying a shift clock pulse to the L2 (slave) latch, placing the scan chain circuit into an operating region, and unloading the scan chain. An additional step may be added to analyze the resulting data. Another method may include the steps of, placing the scan chain circuit into an operating region, loading a scan test pattern into the scan chain circuit, placing the scan chain circuit into a failing region, applying a scan clock pulse to the L1 (master) latch, placing the scan chain circuit into an operating region, applying a shift clock pulse to the L2 latch, and unloading the scan chain. An additional step may be added to analyze the resulting data.